Notice of Allowability	Application No. 10/685,127	Applicant(s) OUYANG ET AL.
	Examiner Toniae M. Thomas	Art Unit 2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the election and amendment received on 20 December 2004*.

2. ☒ The allowed claim(s) is/are *1-20*.

3. ☒ The drawings filed on *14 October 2003* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Mary Wilczewski
Primary Examiner

EXAMINER'S AMENDMENT

1. This action is a first Office action on the merits of Application Serial No. 10/685,127. Claims 1-20 are currently pending.

Election/Restrictions

2. Applicant's election of Group I, claims 21-26, in the reply filed on 20 December 2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)). Nonelected claims 21-26 were cancelled in the amendment filed on 20 December 2004.

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Amendment

4. The application has been amended as follows:

In Specification

In par. 002, line 5,	"(TET)" has been changed to --FET-- after "field effect transistor" and before "flash memory";
In par. 0016, line 2,	"a" has been changed to --at-- after "formed" and before "the same";

In par. 0016, line 6,	"10" has been changed to --12-- before "upper portion";
In par. 0016, line 10,	"filed" has been changed to --field-- after "gate" and before "effect";
In par. 0018, line 5,	--by-- has been inserted after "formed" and before "one";
In par. 0018, line 6,	--when-- has been inserted after, "case" and before "the hardmask";
In par. 0018, line 9,	"is" has been deleted after "SiO_2" and before "thermally";
In par. 0032, line 18,	--be-- has been inserted after "may" and before "carried".

Reasons for Allowance

5. The following is an examiner's statement of reasons for allowance: the prior art of record does not anticipate, teach or suggest a method for an improved polysilicon etching process which forms self-aligned polysilicon micro-integrated circuit structures such that the polysilicon structures are formed without protruding polysilicon portions. For example, the closest prior art of record, Hsu et al. (US 6,569,736 B1), discloses a method for forming self aligned polysilicon micro-integrated circuit structures 54, 50, and 70 in a split-gate flash memory device (figs. 2A-2H and accompanying text). The method comprises the following process steps: providing a semiconductor wafer process

surface 32 comprising first exposed polysilicon portions 50, 54 and adjacent oxide portions 48 (fig. 2C); forming a first oxide layer 46, 56 on the exposed polysilicon portions (fig. 2C); blanket depositing a polysilicon layer 60 on the first exposed polysilicon portions and adjacent oxide portions (fig. 2D and col. 5, lines 61-64); forming a hard mask layer 62 on the polysilicon layer (fig. 2D and col. 5, line 67 - col. 6, line 7); carrying out a multi-step etching process to etch through the hardmask layer and etch through a thickness portion of the polysilicon layer, thereby forming second polysilicon portions 70 adjacent the oxide portions and having upward protruding outer polysilicon fence portions (figs. 2E, 2F, and col. 6, lines 8-20); and carrying out an etching process to remove polysilicon fence portions (fig. 2H and col. 6, lines 26-31). While Hsu discloses carrying out a multi-step etching process to form second polysilicon portions 70 having upward protruding outer polysilicon fence portions, and carrying out an etching process to remove polysilicon fence portions; Hsu lacks anticipation of the following combination of steps substantially as claimed: carrying out a multi-step reactive ion etching (RIE) process to etch through the hardmask layer and through a thickness portion of the polysilicon layer, contacting the semiconductor wafer process surface with an aqueous HF solution, and carrying out a downstream plasma etching process to remove polysilicon fence portions. There is no teaching or suggestion within the prior art of record to modify Hsu by carrying out a multi-step reactive ion etching (RIE) process to etch through the hardmask layer and through a thickness

portion of the polysilicon layer, contacting the semiconductor wafer process surface with an aqueous HF solution, and carrying out a downstream plasma etching process to remove polysilicon fence portions.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday-Thursday from 8:30 a.m. to 5:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TMT
06 March 2005

Mary Wilczewski
Primary Examiner